

Fig. 1A

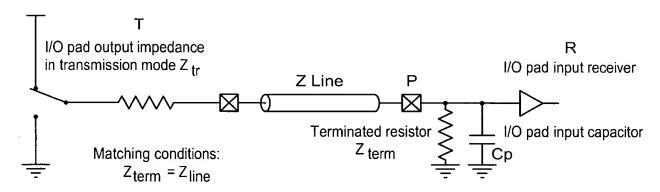
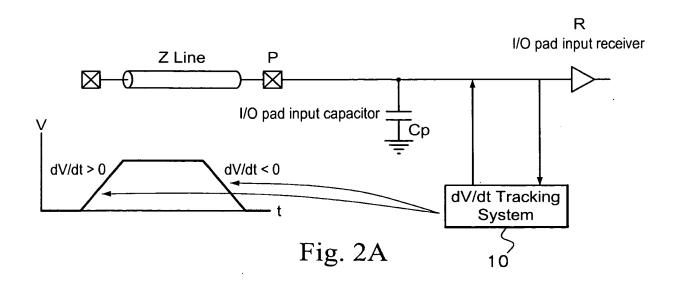


Fig. 1B





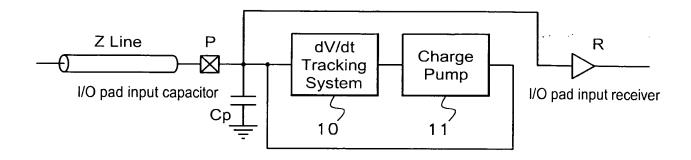


Fig. 2B

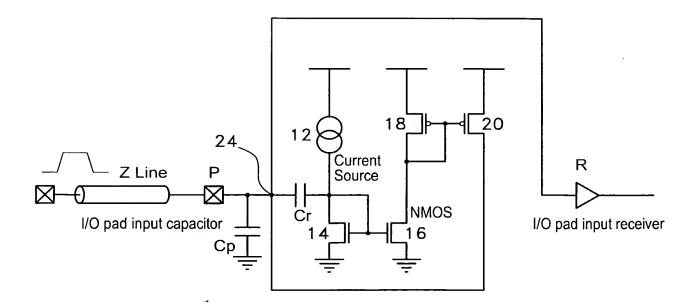
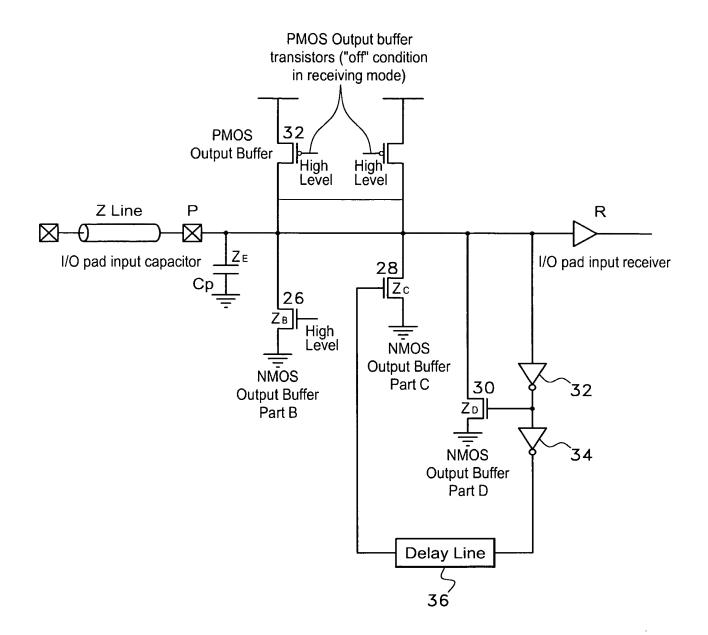


Fig. 2C

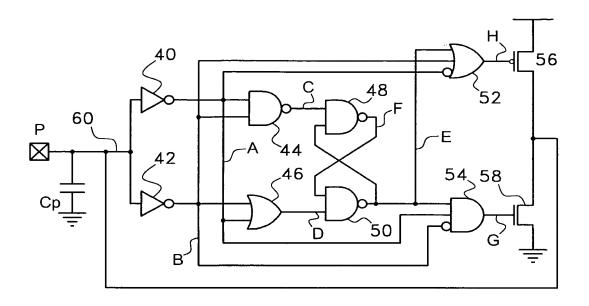




 $Z \ input = ZB \ II \ [ZC \ (or \ ZD \ , \ or \ ZE \)]$ if I ZC I = I ZD I = I ZE I, then an Input signal can not change Z input

Fig. 2D





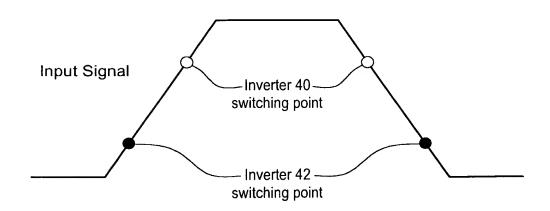


Fig. 3

5/5

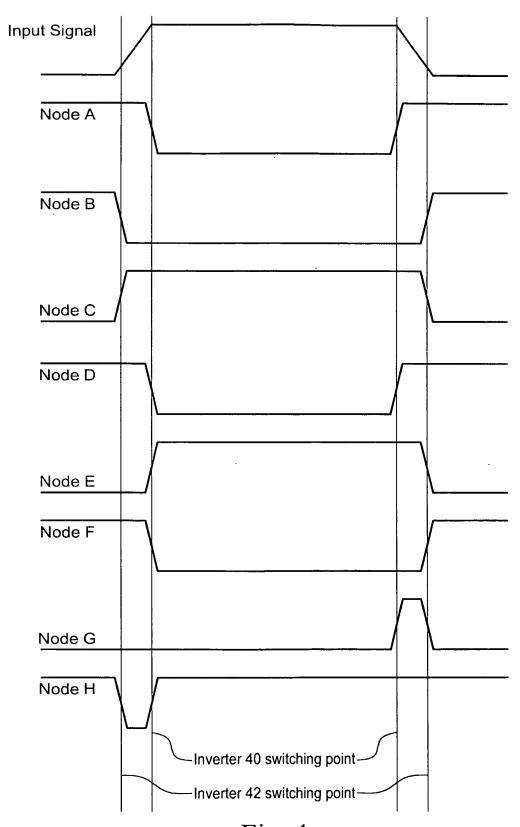


Fig. 4